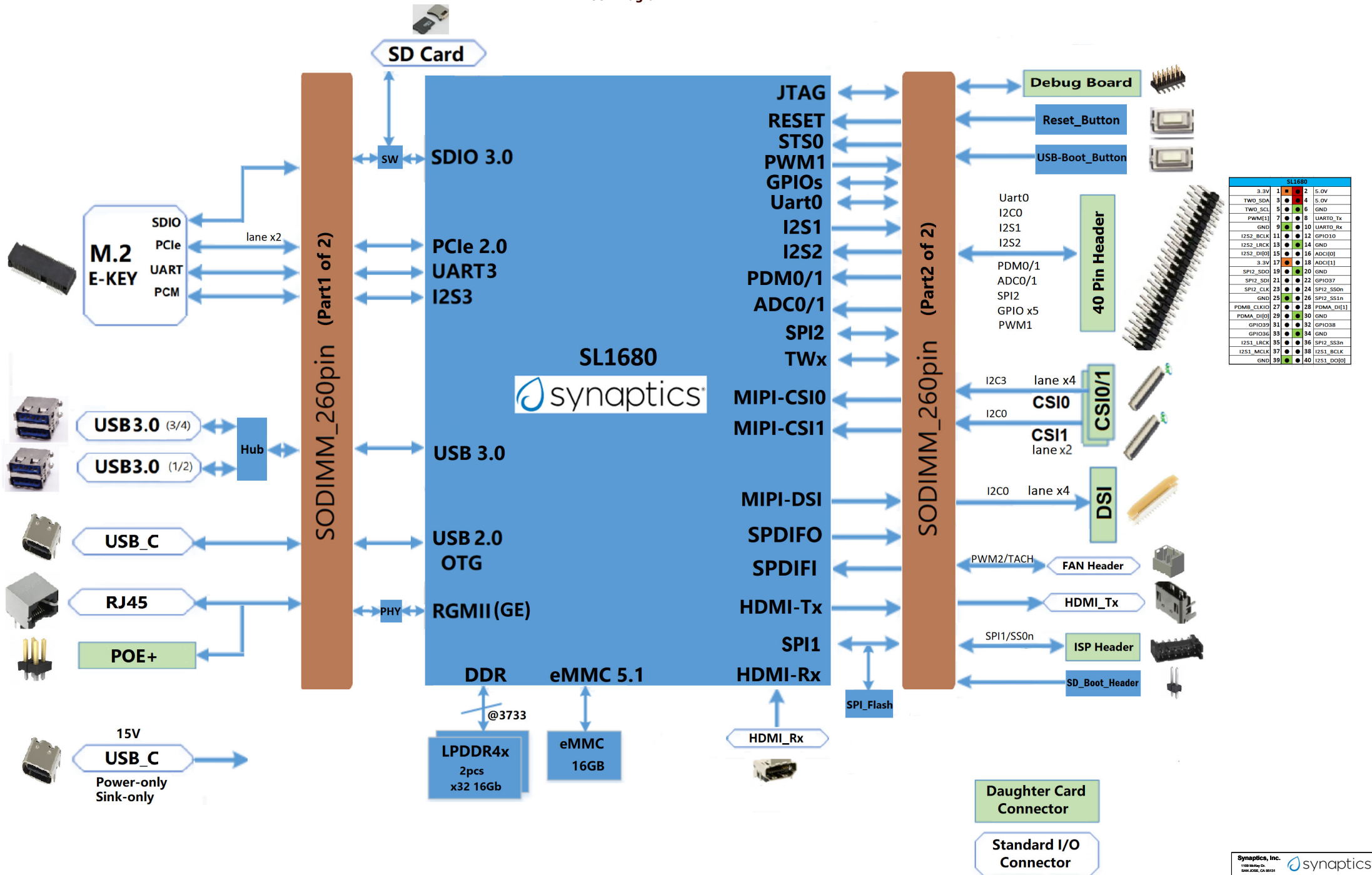


# SL1680 CORE MODULE Schematics

Block Diagram



[illegible]

REVISION HISTORY

Rev#	Date	Originator(s)	Rev Item ID	What Revised	Why Revised	SW Impacts	Other Impacts	Rework# Base On Previous Version	SW Strap [3:1]=b'
A	11/01/2023	William W	1	Preliminary SCH for SL1680	SL1680-RDK design	NO	NO		000
	11/07/2023	William W	2	Update MIPI_DSI, MIPI_CSI0/1 connector and re-defined pin definition.	To fit DSI/CSI popular module in market.				
			3	Update Prefix NetNames to "Soc"	Follow design rule.				
			4	Remove series Capacitor/resistor to I/O-Baord for USB3.0,PCIe, HDMI, Tx signals.	optimize PCB layout				
			5	Short DR directly and use 0201 capacitors/resistor on Ethernet PHY section.	optimize PCB layout				
			6	Update SODIMM-260pin signal fan-out.	optimize PCB layout and fit heatsink holes.				
			7	Update USB-C port for USB2.0 only	USB-C need USB2.0 only.				
			8	Put on-board SPI on Core-Module	Ensure all flashes (eMMC, SPI, SD card) on Core-Module.				
			9	Move standby control to I/O-Board.	Optimize Core-Module layout.				
	11/15/2023	William W	10	Change W25Q128FWSIG to W25Q128JWSIQ, AIC1519N-0 to AP2162A.	Convenience for purchase.				
			11	Change SN74AVC4T245PWR to SN74AVC4T245RSVR; Change TXB0108PWR to TXB0108DQSR; Change 25Mhz crystal footprint from 3.2*2.5mm to 2.0*1.6mm	Small footprint for optimize PCB layout.				
	11/21/2023	William W	12	Change MIPI_CSI0/CSI1 22pin connector to Right-angle	Optimize PCB layout				
	11/23/2023		13	Add ST02, ST03	Fix Core-Module and I/O-Board more robust.				
	11/30/2023		14	Change L68 to SRP1038C-4R7M	The hight of inductor impact bed plate.				
	12/11/2023		15	Change SD-Boot selection by jumper on I/O-Board	Clear for Boot-selection.				
B	01/19/2024	William W	1	Change R189=2.2k from DNS	Keep STRP[SM_SS0] is Low during AC/ON and RESET, avoid external Uart tool impact.	NO	NO	Rework A	000
C	04/10/2024	William W	1	Update Block Diagram with adding SD_Boot_Header	Match with I/O-board changes	Yes	NO	NO	100
			2	Change R1179, R1180, R1181, R1182, R1183, R1184, R1957, R1955 to 33R	EMI improvement				
			3	Change R63 to 22R, mount on R536, C453	EMI improvement				
			4	Add Page-24 for current sensors and do changes accordingly.	Monitor all power rails				
			5	Change R170 to 0R from DNS	Update SW Strap to 3b'100				
D	05/21/2024	William W	1	Update Synaptics Tittle Block	Update Synaptics Tittle Block	NO	NO	NO	100
			2	Change C1341=0.1uF, C1340=1K.	Optimize SD power sequence.				
E	06/28/2024	William W	1	Update power test pads to 40mil from 18mil	Manufacturer requirement	NO	NO	NO	100
			2	Add 4 standoffs for mounting Heatsink	Manufacturer requirement				

# SL1680 RDK I/O Reference

For details, please refer to  
SL1680\_RDK\_IO\_reference.xlsx;

- \*\* Pinmux for Standard Interface sheet
- \*\* Pinmux for GPIO sheet
- \*\* GPIO Expander over I2C sheet
- \*\* I2C Bus sheet

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Title

**04: PIN-DeMUX TABLE**

Size

Document Number

**SC950-000797-01**

Rev

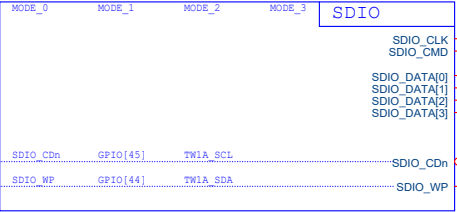
**E**

Date: Tuesday, July 09, 2024

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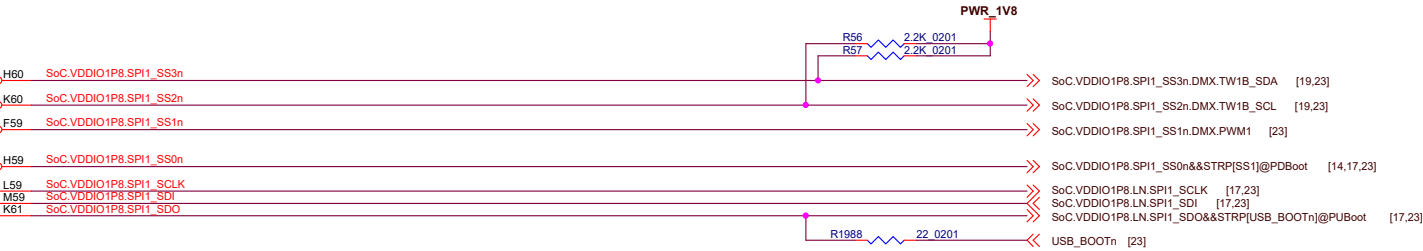
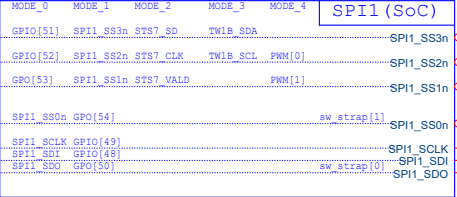


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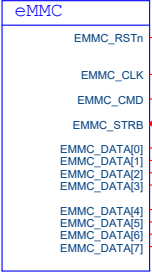
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U1-6



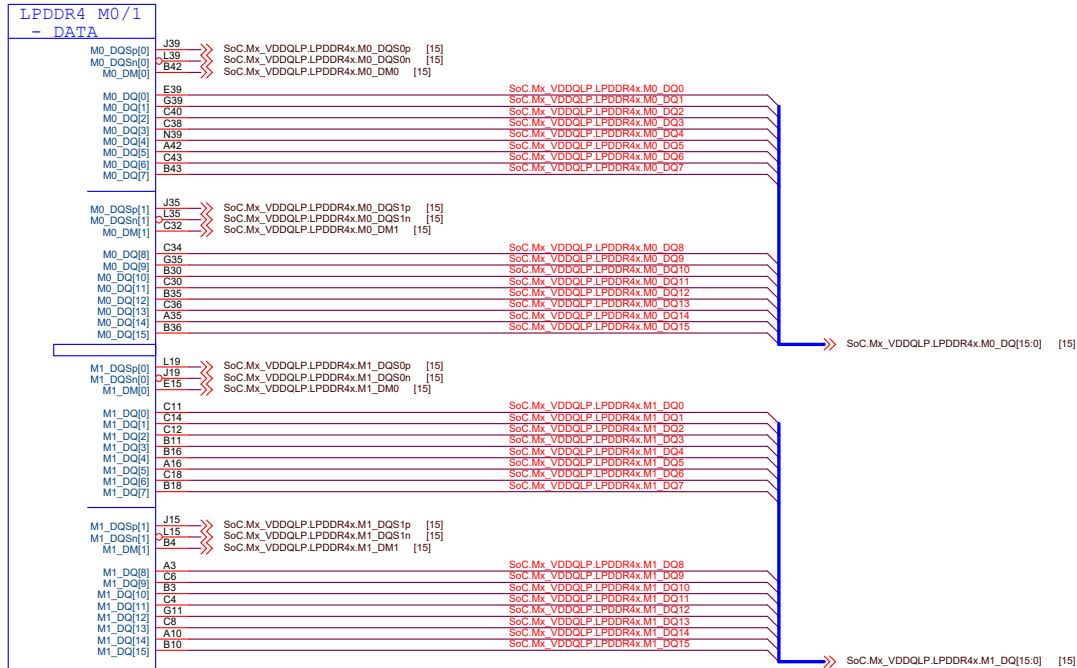
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U1-8

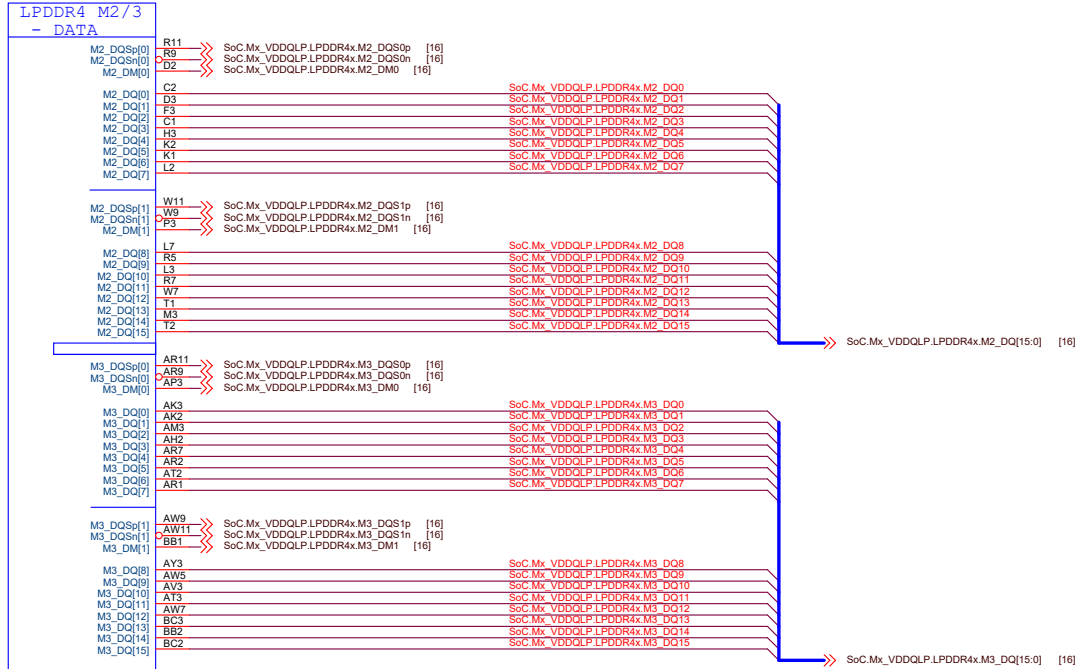


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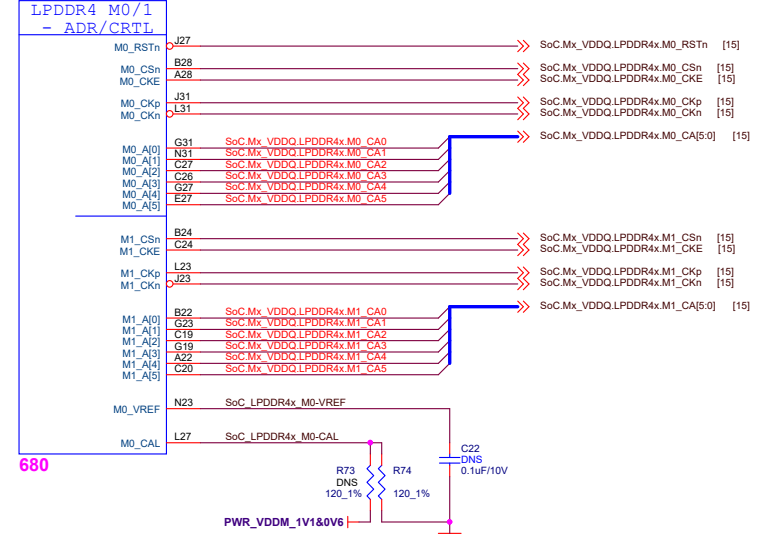
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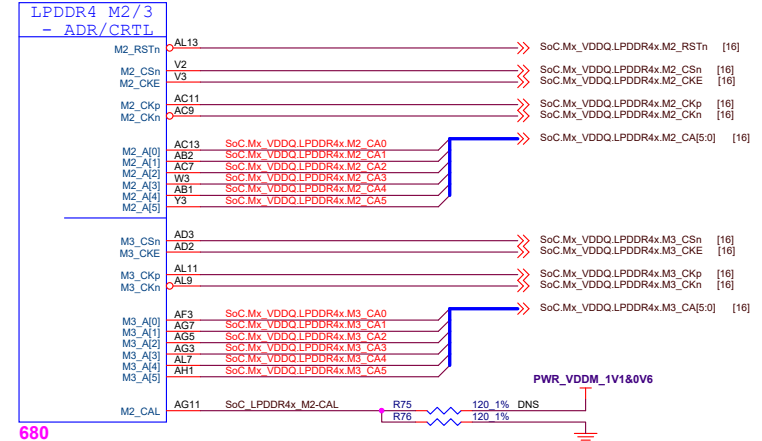
## U1-5



## U1-2



## U1-4



```

MODE_0  MODE_1  MODE_2  MODE_3  MODE_4  T2S
GPIO[18]  I2S1_MCLK  STS2_SOP  I2S1_MCLK
GPIO[20]  I2S1_BCLKIO PWM[1]  I2S1_BCLK
GPIO[21]  I2S1_LCKIO PWM[0]  ARC_TEST_OUT  I2S1_LCK
GPIO[19]  I2S1_DO[0]  I2S1_DO[0]
GPIO[17]  I2S1_DI[0]  STS2_CLK  I2S1_DI[0]
GPIO[16]  I2S1_DO[2]  PWM[2]  STS2_SD  PWMB_DI[2]  I2S1_DO[2]
GPIO[15]  I2S1_DO[3]  PWM[3]  STS2_VALID  PWMB_DI[3]  I2S1_DO[3]

GPIO[7]  I2S2_MCLK  PWMB_CLKIO  HDMI_FBCLK  strap
boot_src[0]  I2S2_MCLK
GPIO[12]  I2S2_BCLKIO  PWMB_CLKIO  I2S2_BCLK
GPIO[13]  I2S2_LCKIO  I2S2_LCK
GPIO[11]  I2S2_DI[0]  PWMB_DI[3]  I2S2_DI[0]
GPIO[10]  I2S2_DI[1]  PWMB_DI[2]  STS4_VALID  I2S2_DI[1]

GPIO[9]  I2S2_DI[2]  PWMB_DI[1]  STS4_CLK  I2S2_DI[2]
GPIO[8]  I2S2_DI[3]  PWMB_DI[0]  STS4_SOP  I2S2_DI[3]

GPIO[4]  SPDIF1  PWMC_DI  SPDIF1

GPIO[14]  SPDIF0  AVPLL_CLK  boot_src[1]  SPDIF0
GPIO[3]  I2S3_LCKIO  STS3_CLK  I2S3_LCK
GPIO[2]  I2S3_BCLKIO  STS3_SD  I2S3_BCLK
GPIO[6]  I2S3_DI  STS3_VALID  I2S3_DI
GPIO[1]  I2S3_DO  STS3_SOP  I2S3_DO


```

MODE_0	MODE_1	MODE_3	strap	RGMI_I
RGMI_MDC	GPIO[29]			RGMI_MDC
RGMI_MDIO	GPIO[28]			RGMI_MDIO
RGMI_TXCTL	GPIO[22]		pllbyts	RGMI_TXCTL
RGMI_TXC	GPIO[23]		legacy boot	RGMI_TXC
RGMI_TXD[0]	GPIO[27]		sw_strap[2]	RGMI_TXD[0]
RGMI_TXD[1]	GPIO[26]		sw_strap[3]	RGMI_TXD[1]
RGMI_TXD[2]	GPIO[25]		cpuArbByte	RGMI_TXD[2]
RGMI_TXD[3]	GPIO[24]		pllPerDown	RGMI_TXD[3]
RGMI_RXCTL	GPIO[30]			RGMI_RXCTL
RGMI_RXC	GPIO[31]			RGMI_RXC
RGMI_RXD[0]	GPIO[35]			RGMI_RXD[0]
RGMI_RXD[1]	GPIO[34]			RGMI_RXD[1]
RGMI_RXD[2]	GPIO[33]			RGMI_RXD[2]
RGMI_RXD[3]	GPIO[32]			RGMI_RXD[3]

MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	STS
GPIO[43]	STSD_CLK	CPUPPL_CLKO		URT3_RAO	
GPIO[42]	STSD_SOP	STSPPL_CLKO	STSS_CLK	URT3_TAO	STSD_CLK
GPIO[41]	STSD_SD	STSPPL_CLKO		URT3_CSTN	STSD_SOP
GPIO[40]	STSD_VALD		STSS_SD	URT3_STSN	STSD_SD
					STSD_VALD
GPIO[39]	STSI_CLK	PWM[0]			STSI_CLK
GPIO[38]	STSI_SOP	PWM[1]	STSG_CLK		STSI_SOP
GPIO[37]	STSI_SD	PWM[2]			STSI_SD
GPIO[36]	STSI_VALD	PWM[3]	STSG_SD		STSI_VALD

T80	SoC.VDDIO1P8.RGMII_MDC		SoC.VDDIO1P8.LN.RGMII_MDC	[18]
W55	SoC.VDDIO1P8.RGMII_MDIO		SoC.VDDIO1P8.LN.RGMII_MDIO	[18]
AC51	SoC.VDDIO1P8.LN.RGMII_TXCTL		SoC.VDDIO1P8.LN.RGMII_TXCTL&&STRP[pIIBysp]@PDBoot	[14,18]
T61	SoC.VDDIO1P8.LN.RGMII_TXC		SoC.VDDIO1P8.LN.RGMII_TXC&&STRP[egacy_boot]@PDBoot	[14,18]
V59	SoC.VDDIO1P8.LN.RGMII_TXD0		SoC.VDDIO1P8.LN.RGMII_TXD0&&STRP[SS2]@PUBoot	[14,18]
A647	SoC.VDDIO1P8.LN.RGMII_TXD1		SoC.VDDIO1P8.LN.RGMII_TXD1&&STRP[SS3]@PUBoot	[14,18]
W59	SoC.VDDIO1P8.LN.RGMII_TXD2		SoC.VDDIO1P8.LN.RGMII_TXD2&&STRP[pwRbysp]@PDBoot	[14,18]
Y59	SoC.VDDIO1P8.LN.RGMII_TXD3		SoC.VDDIO1P8.LN.RGMII_TXD3&&STRP[pwRDown]@PDBoot	[14,18]
AC55	SoC.VDDIO1P8.RGMII_RXCTL		SoC.VDDIO1P8.RGMII_RXCTL	[18]
AG49	SoC.VDDIO1P8.RGMII_RXC		SoC.VDDIO1P8.RGMII_RXC	[18]
AC53	SoC.VDDIO1P8.RGMII_RXD0		SoC.VDDIO1P8.RGMII_RXD0	[18]
AB61	SoC.VDDIO1P8.RGMII_RXD1		SoC.VDDIO1P8.RGMII_RXD1	[18]
T60	SoC.VDDIO1P8.RGMII_RXD2		SoC.VDDIO1P8.RGMII_RXD2	[18]
AG51	SoC.VDDIO1P8.RGMII_RXD3		SoC.VDDIO1P8.RGMII_RXD3	[18]

MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	STS
GPIO[43]	STSP_CLK	CPUPPL_CLKO		URT3_RXD	
GPIO[42]	STSP_CLK	STSPCLK_CLKO	STSP5_CLK	URT3_TXD	STSP0_CLK
GPIO[41]	STSP_SD	MEMPLP_CLKO		URT3_CTS	STSP0_SOP
GPIO[40]	STSP_VALD		STSP5_SD	URT3_RTSn	STSP0_SD
					STSP0_VALD
<hr/>					
GPIO[39]	STSP1_CLK	PWM[0]			STSP1_CLK
GPIO[38]	STSP1_SOP	PWM[1]	STSP6_CLK		STSP1_SOP
GPIO[37]	STSP1_SD	PWM[2]			STSP1_SD
GPIO[36]	STSP1_VALD	PWM[3]	STSP6_SD		STSP1_VALD

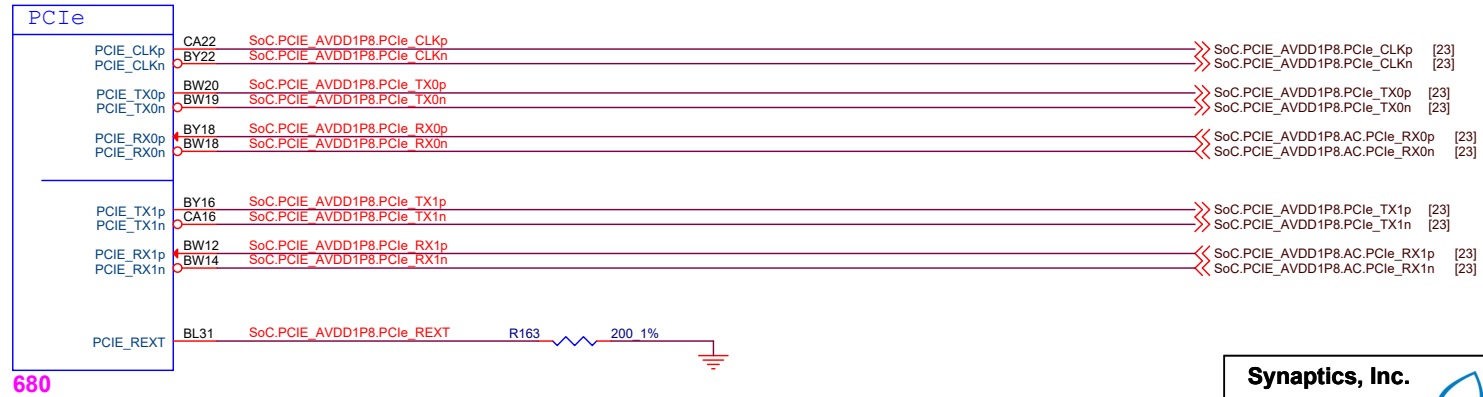
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<b>Title</b> 08: 12S/SPDIF,RGMII,STS					
<b>Size</b>	<b>Document Number</b> SC950-000797-01				<b>Rev</b> E
<b>Date:</b>	Tuesday, July 09, 2024		Sheet	8	of 24



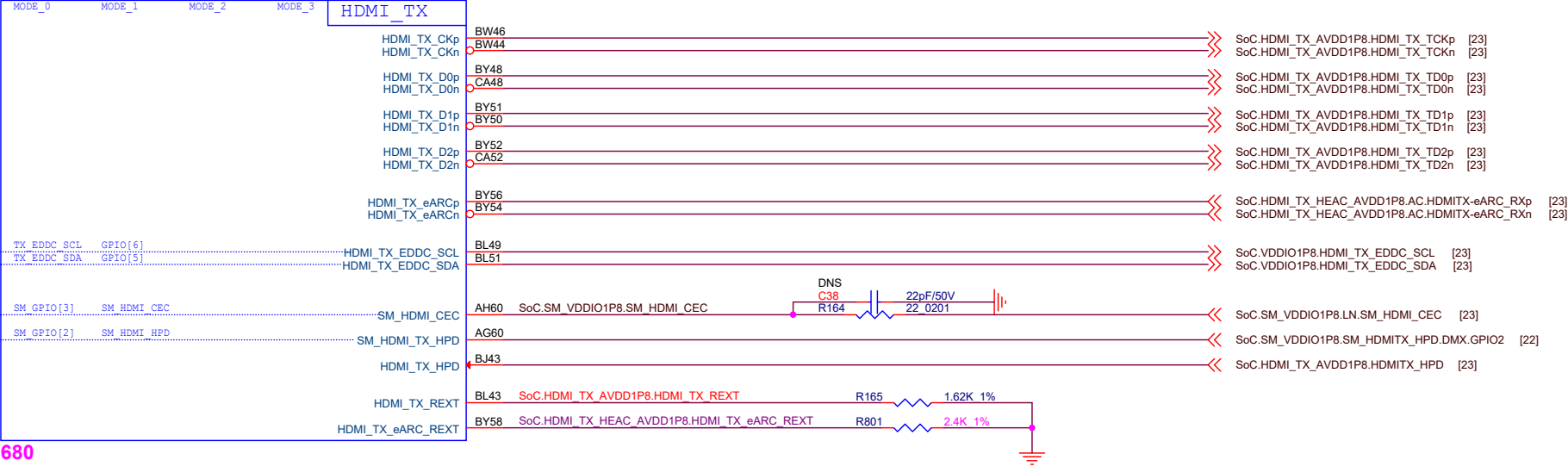
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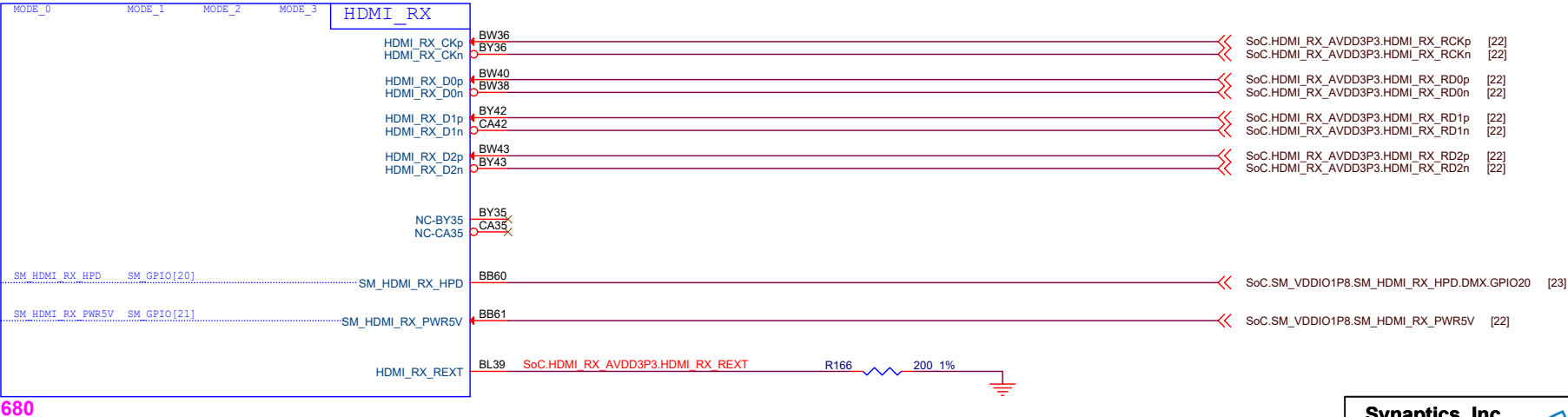
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U1-13

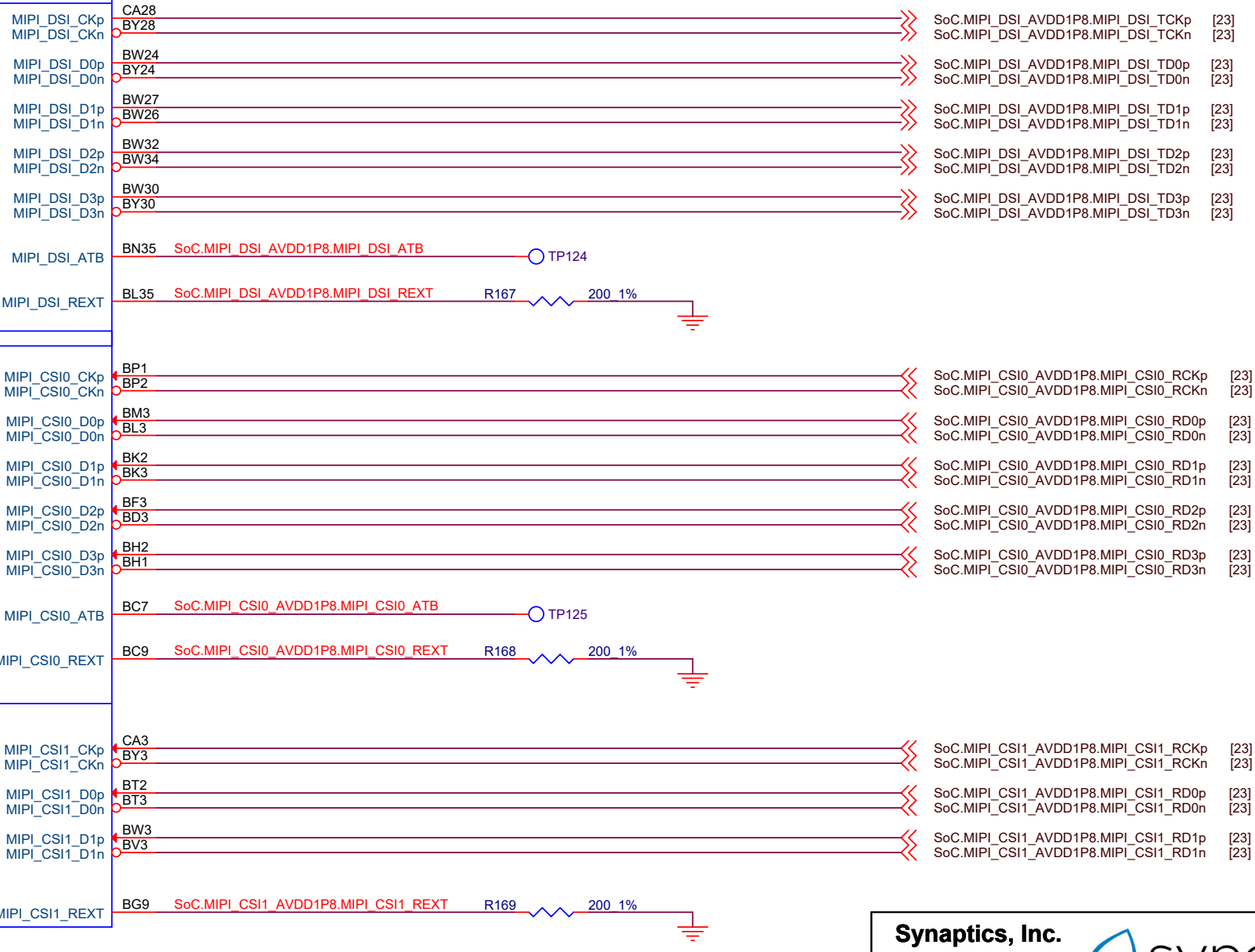


U1-14



# U1-17

## MIPI



680

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Title		
11: MIPI DSI/CSI		
Size	Document Number	Rev
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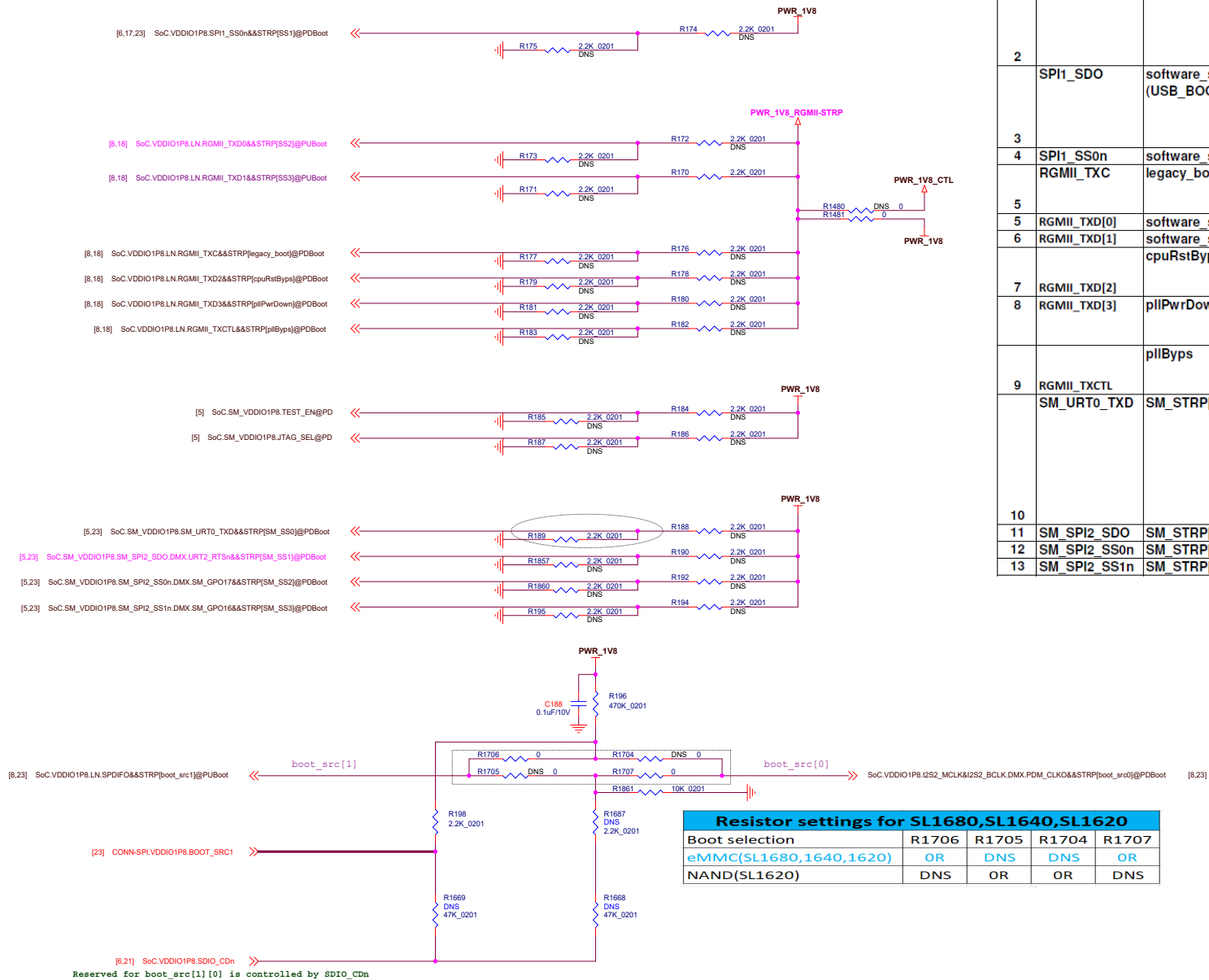


## POWER



GND

680



S.No	Pad Name	Strap name	Description	on-chip PU/PD
1	SPDIFO	boot_src[1]	CPU Boot Source bit[1]	PU
	I2S2_MCLK	boot_src[0]	CPU boot source bit[0]: 00: ROM boot from SPI 01: Reserved 10: ROM boot from EMMC 11: Direct boot from SPI(Only available when ENG_EN=1) When direct boot from SPI(SPI clear boot), pwrCntlByps and cpuRstByps should be set to 1, plIByps Strap should be set to 0, plIPwrDown should be set to 0	PD
2	SPH1_SDO	software_strap[0] (USB_BOOTn)	Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB 1: Boot from the device select by boot_src	PU
3	SPH1_SS0n	software_strap[1]	Straps for software usage	PD
4	RGMII_TXC	legacy_boot	Strap to reduce reset wait time 0: 2ms 1: 20ms	PD
5	RGMII_TXD[0]	software_strap[2]	Straps for software usage	PD
6	RGMII_TXD[1]	software_strap[3]	Straps for software usage	PD
7	RGMII_TXD[2]	cpuRstByps	CPU reset bypass strap 0: Enable reset logic inside cpu partition 1: Bypass reset logic inside cpu partition	PD
8	RGMII_TXD[3]	plIPwrDown	SYS/MEM/CPU PLL Power Down 1: Power Down 0: Power UP	PD
9	RGMII_TXCTL	plIByps	SYS/MEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed	PD
10	SM_URT0_TXD	SM_STRP[0]	SM to SOC RSTn mode select 0: socRstN releasing waits for SoCRstCnt but does not wait for SM_PWR_OK(mode_0 of SM_URT0_TXD, system will assert this signal when SOC core power is ready). 1: socRstN releasing waits for both SoCRstCnt and SM_PWR_OK.	PD
11	SM_SPI2_SDO	SM_STRP[1]	software strap	PD
12	SM_SPI2_SS0n	SM_STRP[2]	software strap	PD
13	SM_SPI2_SS1n	SM_STRP[3]	software strap	PD

# U9A

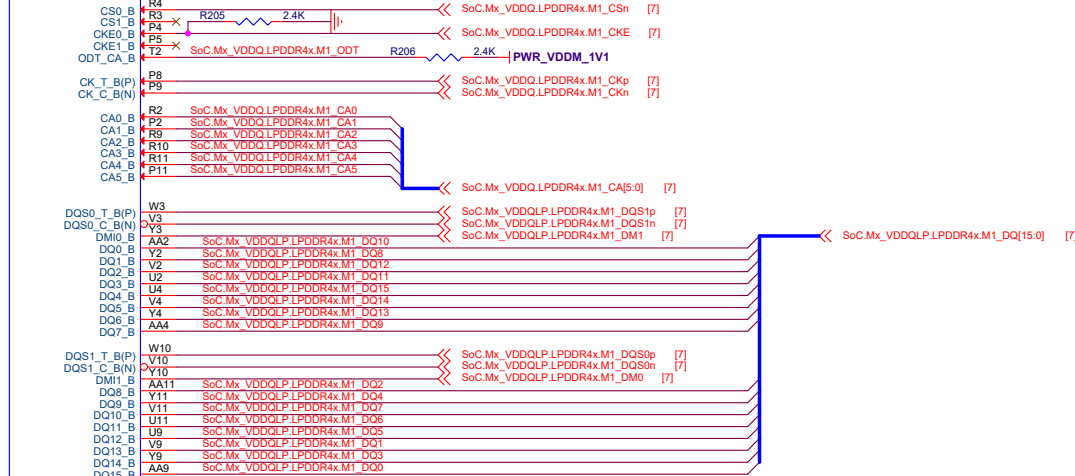
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MT53D512M32D2DS-053 AIT:D

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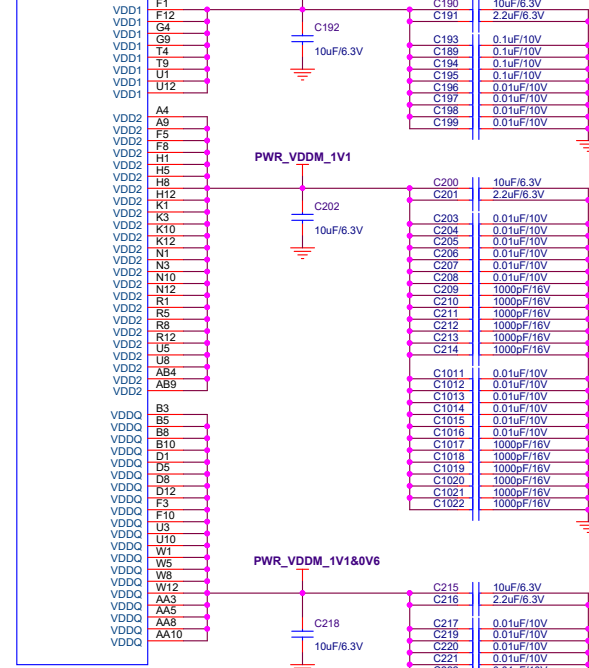
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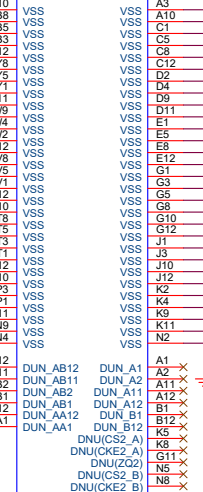
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MT53D512M32D2DS-053 AIT:D

# U9D

## SDRAM GND



MT53D512M32D2DS-053 AIT:D

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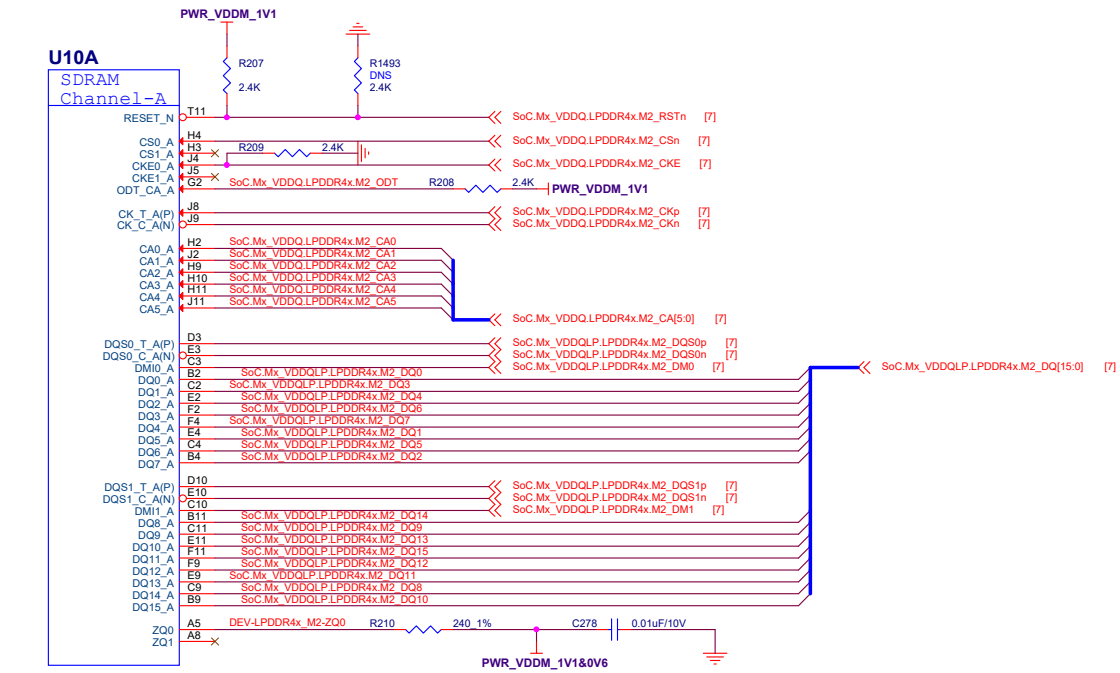
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**SC950-000797-01**

Date: Tuesday, July 09, 2024

Rev  
**E**

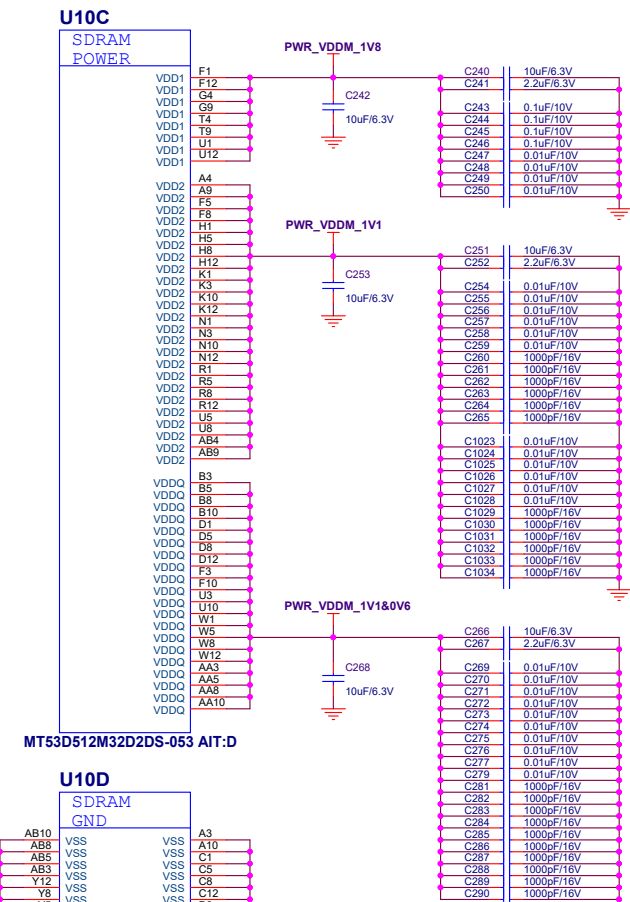
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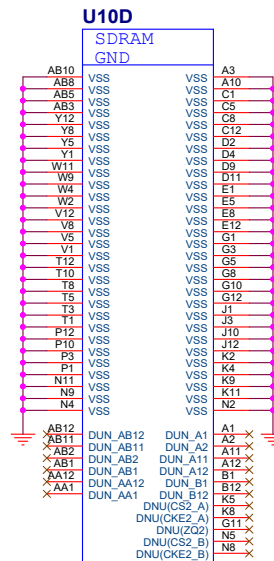
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MT53D512M32D2DS-053 AIT:D



MT53D512M32D2DS-053 AIT:D



MT53D512M32D2DS-053 AIT:D



[6] SoC.EMMC\_VDDIO18.eMMC\_RSTn  
[6] SoC.EMMC\_VDDIO18.eMMC\_CLK  
[6] SoC.EMMC\_VDDIO18.eMMC\_CMD  
[6] SoC.EMMC\_VDDIO18.eMMC\_STRB

[6] SoC.EMMC\_VDDIO18.eMMC\_DATA[7:0]

SoC.EMMC\_VDDIO18.eMMC\_RSTn  
SoC.EMMC\_VDDIO18.eMMC\_CLK  
SoC.EMMC\_VDDIO18.eMMC\_CMD  
SoC.EMMC\_VDDIO18.eMMC\_STRB  
SoC.EMMC\_VDDIO18.eMMC\_DATA0  
SoC.EMMC\_VDDIO18.eMMC\_DATA1  
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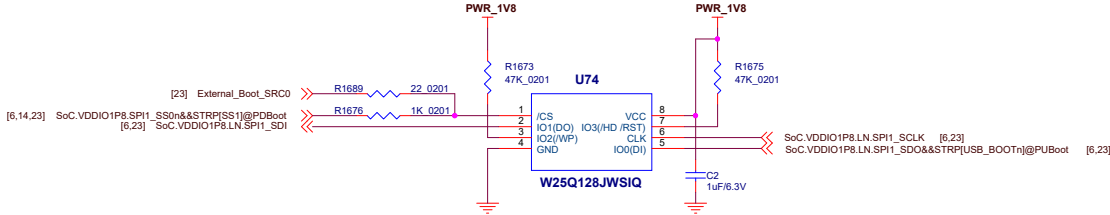
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eMMC\_DATA4  
eMMC\_DATA5  
eMMC\_DATA6  
eMMC\_DATA7

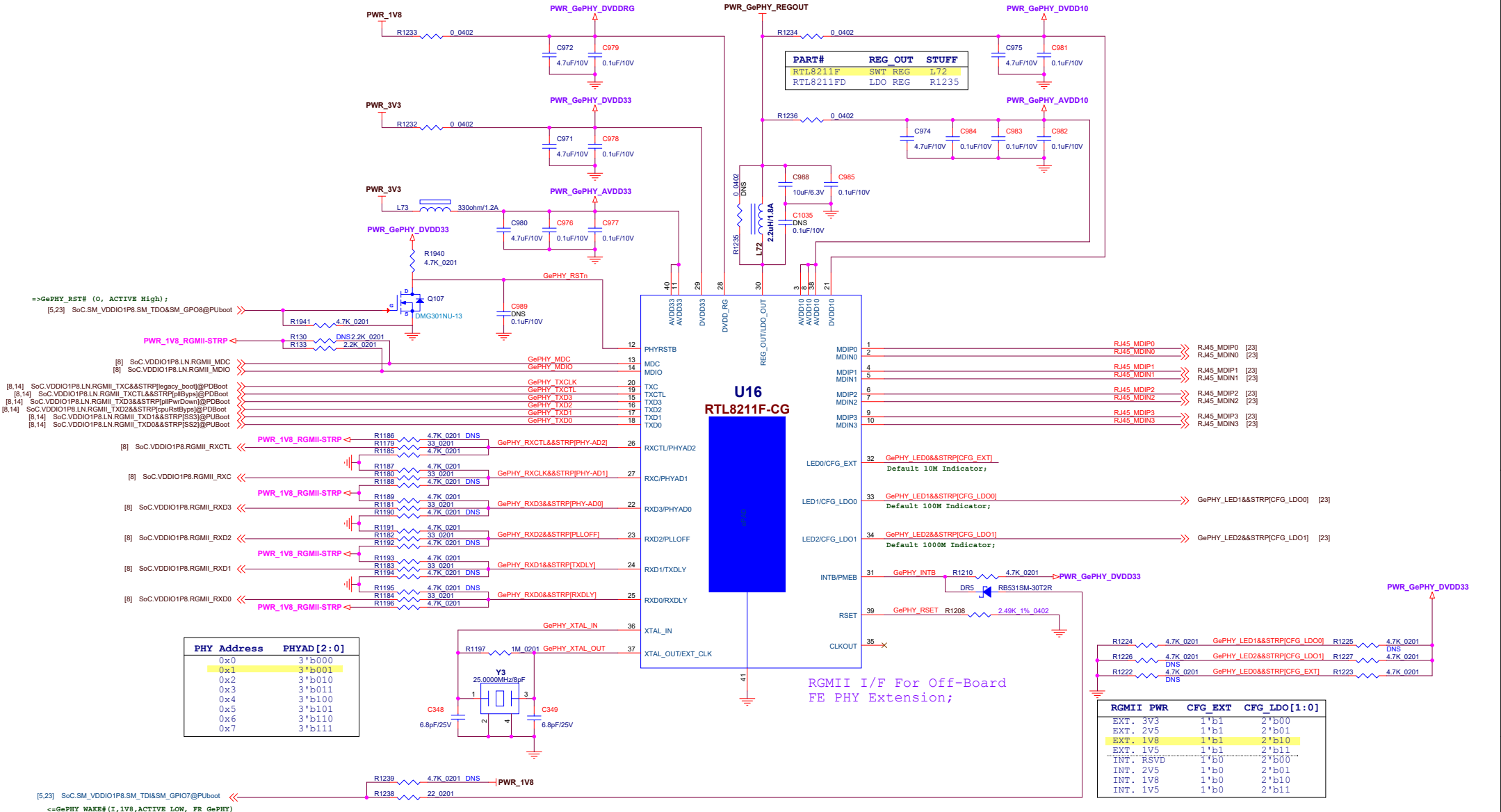
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G2 RFU\_2  
G3 RFU\_3  
K6 RFU\_4  
K7 RFU\_5  
K10 RFU\_6  
P7 RFU\_7  
P10 RFU\_8  
E9 RFU\_9  
E10 RFU\_10  
F10 RFU\_11  
F10 RFU\_12

H1 NC\_H1  
H2 NC\_H2  
H3 NC\_H3  
H12 NC\_H12  
H13 NC\_H13  
H14 NC\_H14  
J1 NC\_J1  
J2 NC\_J2  
J3 NC\_J3  
J12 NC\_J12  
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N14 NC\_N14  
P1 NC\_P1  
P2 NC\_P2  
P6 NC\_P6  
P9 NC\_P9  
P11 NC\_P11  
P12 NC\_P12  
P13 NC\_P13  
P14 NC\_P14

MTFC16GAPALBH-IT TR

A1 NC\_A1  
A2 NC\_A2  
A8 NC\_A8  
A9 NC\_A9  
A10 NC\_A10  
A11 NC\_A11  
A12 NC\_A12  
A13 NC\_A13  
A14 NC\_A14  
B1 NC\_B1  
B7 NC\_B7  
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B9 NC\_B9  
B10 NC\_B10  
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G13 NC\_G13  
G14 NC\_G14





## Default 0.8V/6A for SOC VDD\_CORE;

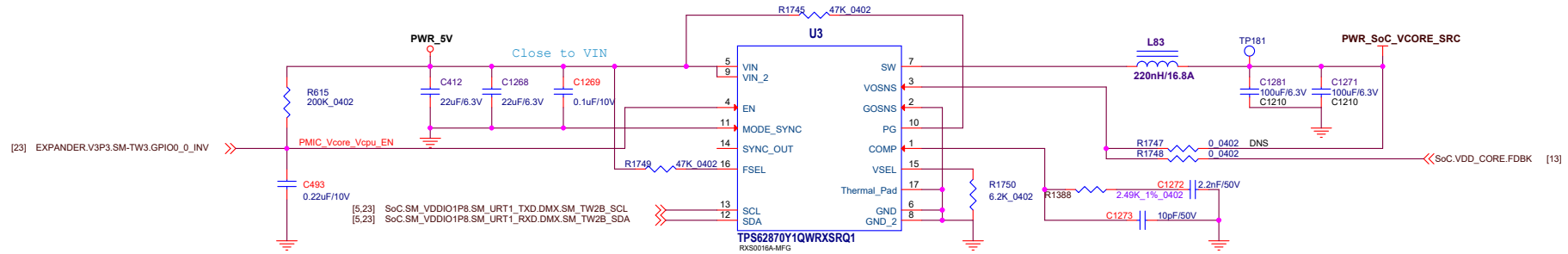


Table For 6A and 9A PMIC

Current	P/N#	Freq	Slave Add(7-bit)	Cout	L
6A	TPS62870Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	220nH (XAL4020-221MEC)
9A	TPS62871Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	100nH (IHLP2020CZERR10M11)

6A: R1388=2.49K

9A: R1388=1.78K

## Default 0.8V/6A for SOC VDD\_CPU;

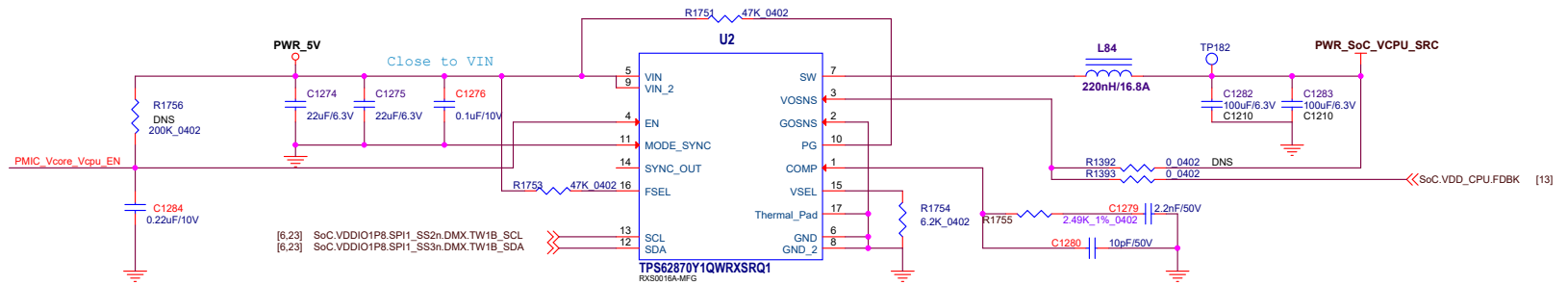


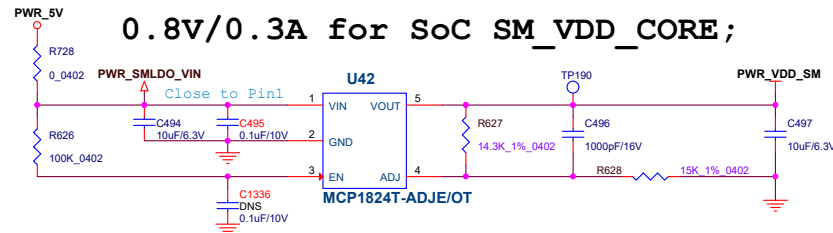
Table For 6A and 9A PMIC

Current	P/N#	Freq	Slave Add(7-bit)	Cout	L
6A	TPS62870Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	220nH (XAL4020-221MEC)
9A	TPS62871Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	100nH (IHLP2020CZERR10M11)

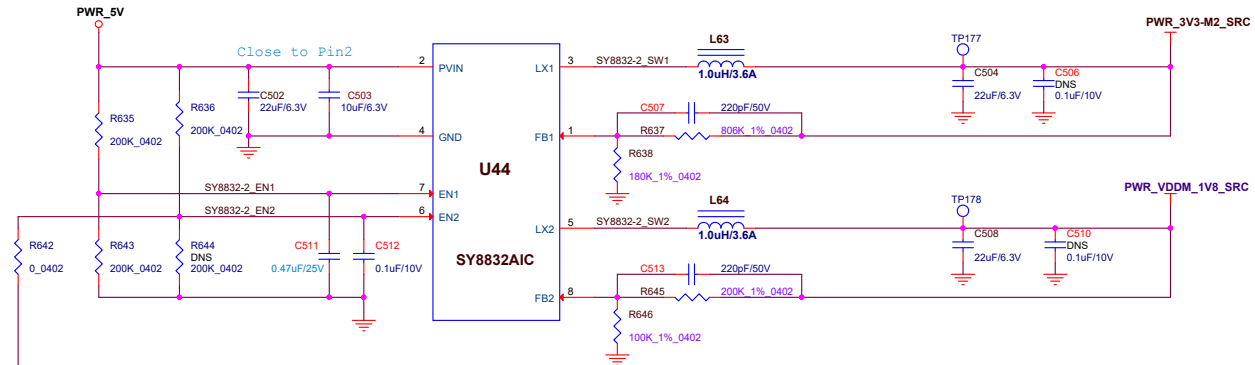
6A: R1755=2.49K

9A: R1755=1.78K

## 0.8V/0.3A for SoC SM\_VDD\_CORE;



### 3.3V/2A & 1.8V/2A for M.2 & DDR-SOC+DDR-DEVICES\_VDD1(1.8V) ;

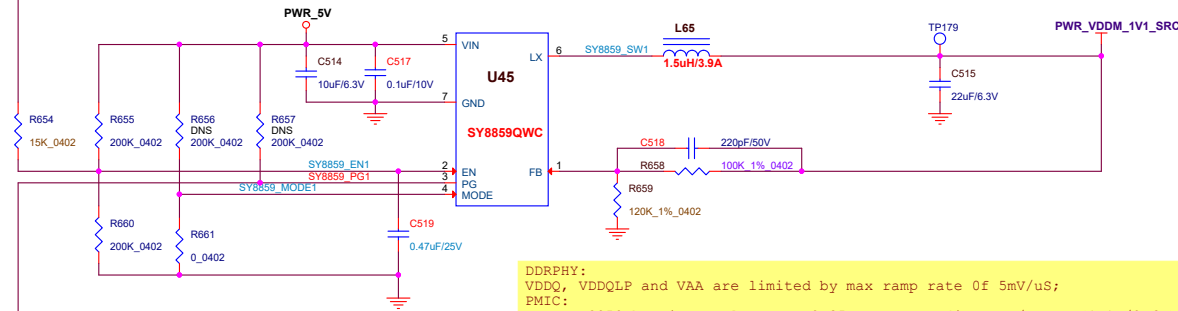


[23] EXPANDER.V3P3.SM-TW3.GPIO0\_2\_INV

### 1.1V/3A for DDR-SOC+DDR-DEVICES\_VDD2(1.1V)

PMIC	Inductor(L)	Cout Stuffing(22uF x4 max, L=1.5uH)
SY8859QWC	1.5uH	1pcs@PMIC & 1pcs@SoC_PHY+2pcs@DEVs

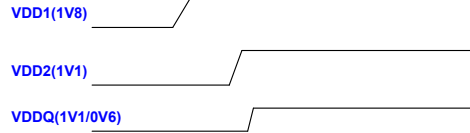
DDR\_1V1/1V8/3V3  
Voltage ON Indicator



#### LPDDR4x Power supply voltage ramp requirements:

- 1)VDD1 must ramp at the same time or earlier than VDD2.
- 2)VDD2 must ramp at the same time or earlier than VDDQ.  
i.e., VDD1>=VDD2>=VDDQ on power-up sequence.

#### Power-Up Sequence For LPDDR4x DEVICE



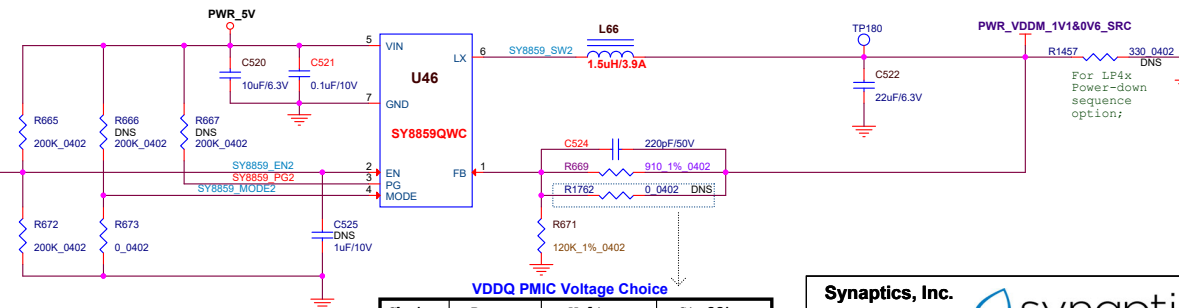
#### Power for proper Self Refresh operation:

- 1)Power supply pins (VDD1, VDD2 and VDDQ) must be at valid levels.
- 2)VDDQ may be turned off during Self-Refresh with Power Down after tCKELCK(Max(5ns,5nCK)) is satisfied (Refresh to figure about tCKELCK). Prior to exiting Self-Refresh with Power Down, VDDQ must be within specified limits.

[23] EXPANDER.V3P3.SM-TW3.GPIO0\_3\_INV

### 1.1V(0.6V)/3A for DDR-SOC+DDR-DEVICES\_VDDQ(1.1V/0.6V)

PMIC	Inductor(L)	Cout Stuffing(22uF x4 max, L=1.5uH)
SY8859QWC	1.5uH	1pcs@PMIC & 1pcs@SoC_PHY+2pcs@DEVs



Choice	Rpu	Voltage	Stuffing
1	910	0.60V	Default
2	100K	1.10V	Option

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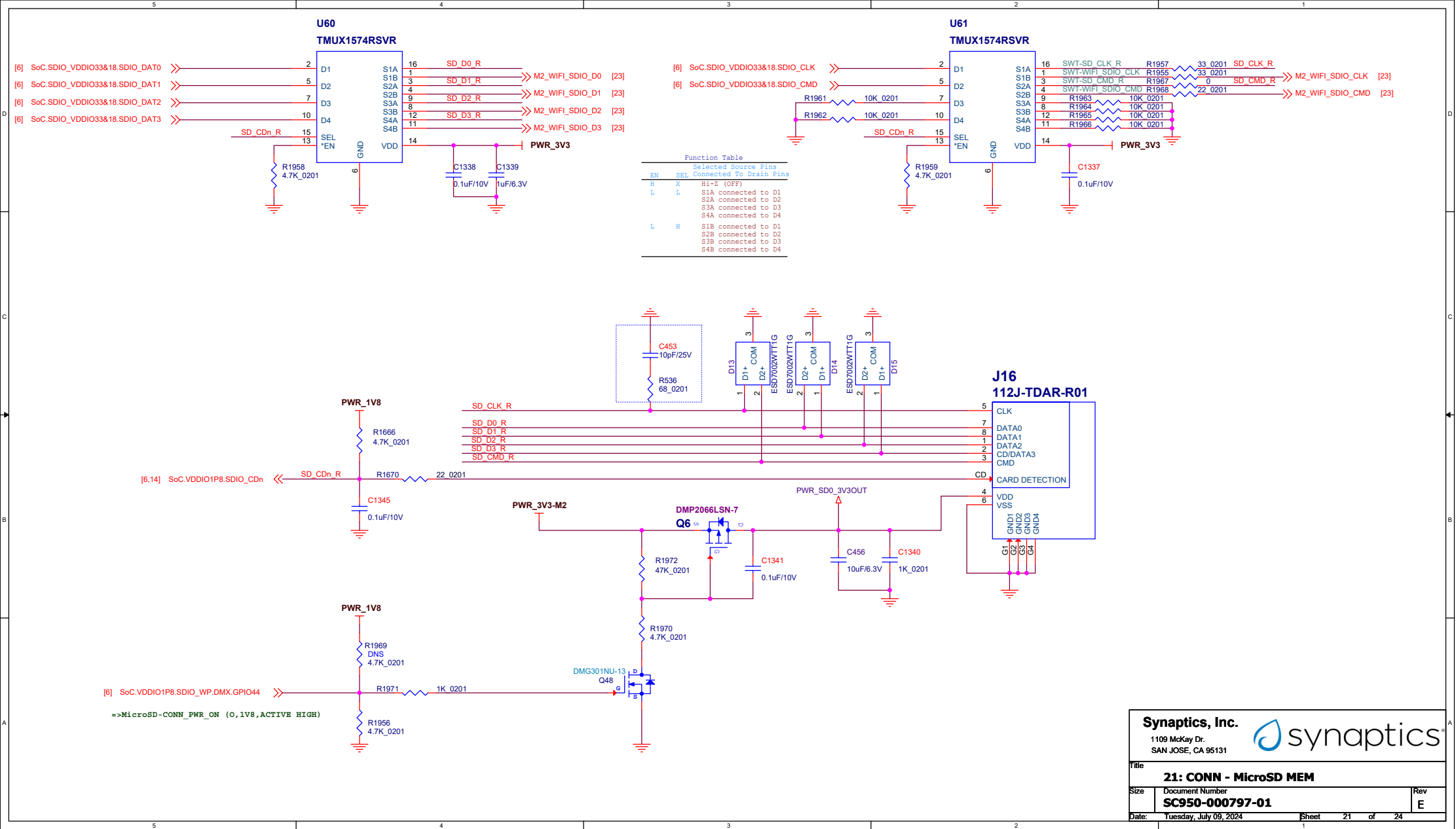
Title: **20: PWR-VDDM\_1V8/1V1/0V6,M2\_3V3**

Size: Document Number **SC950-000797-01**

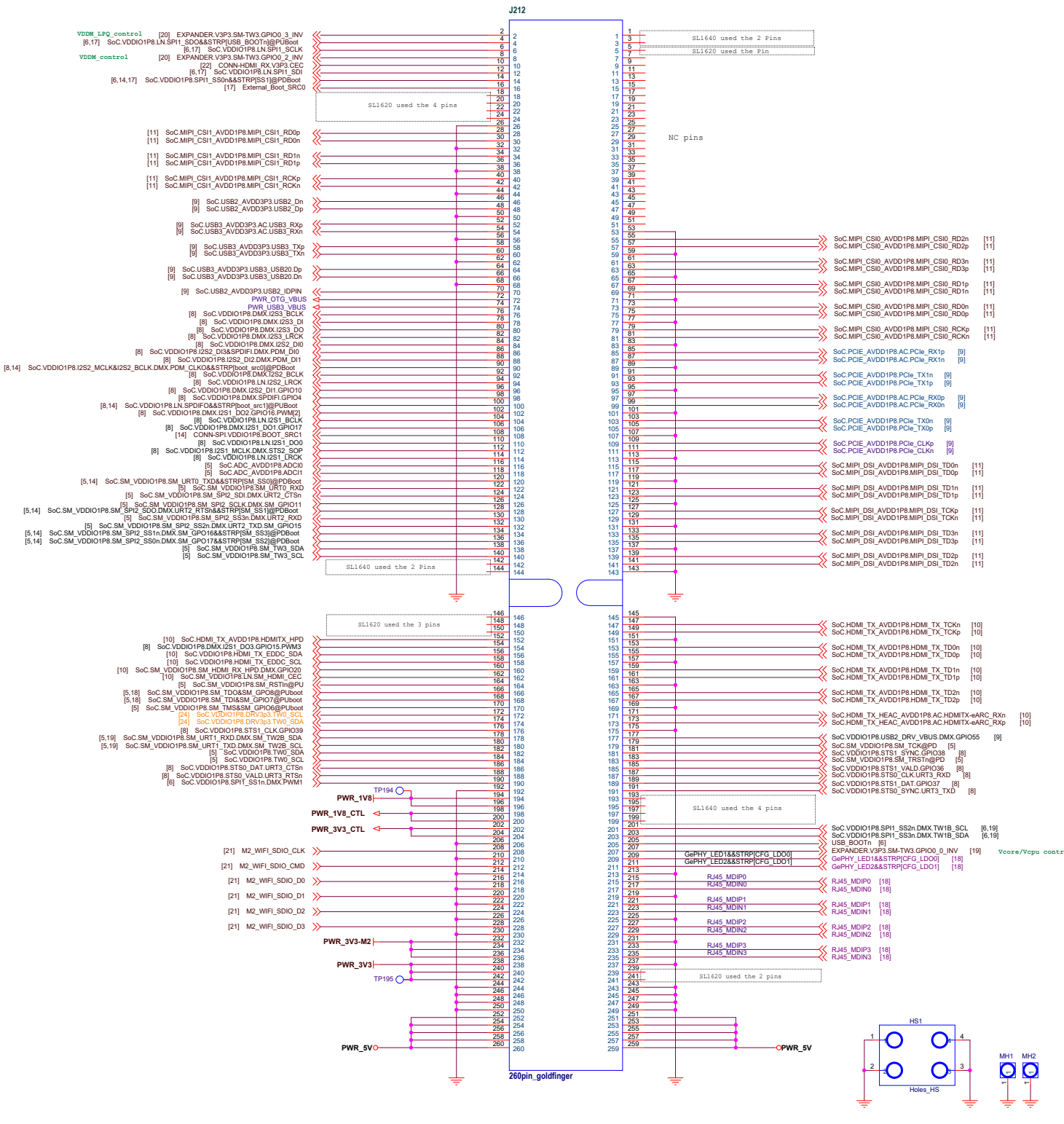
Date: Tuesday, July 09, 2024

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Rev E







**Overlap with Holes HS**

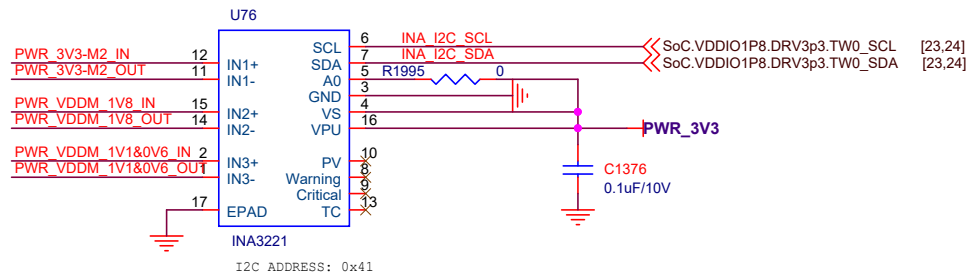
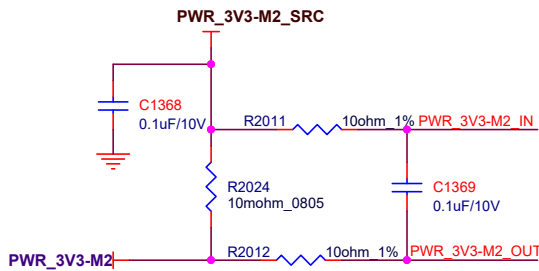
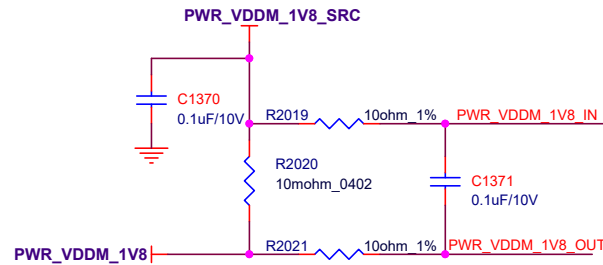
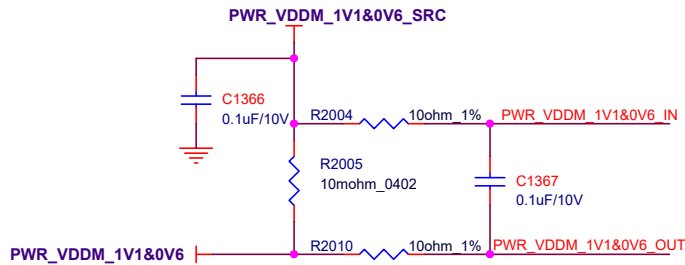
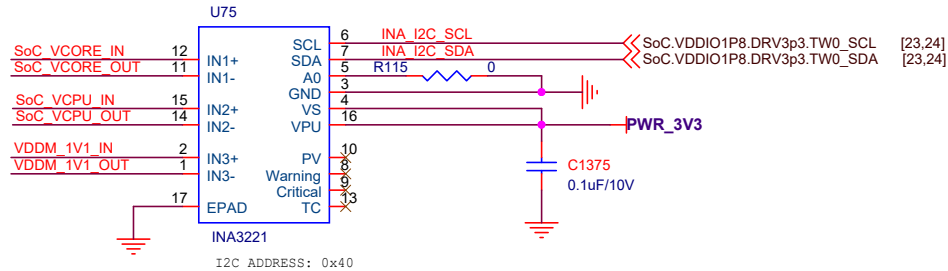
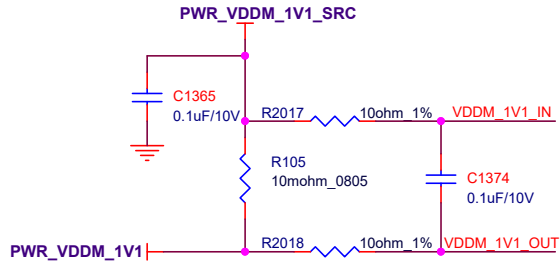
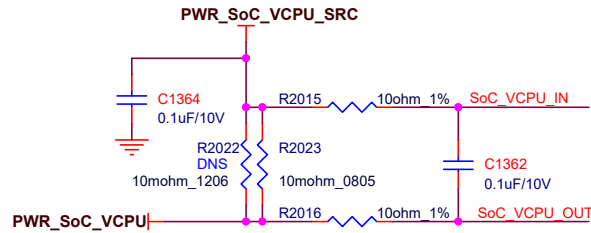
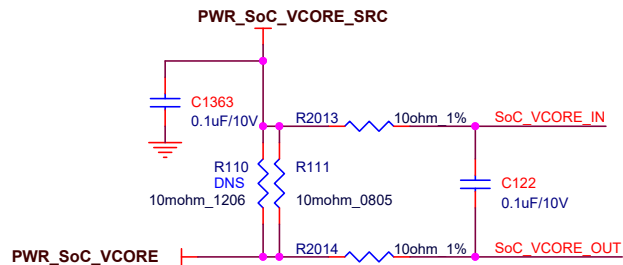
STO1 STO2 STO3 STO4  
StandOff StandOff StandOff StandOff

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**23: SODIMM\_260P\_Goldfinger**

Size: Document Number: **SC950-000797-01** Rev: E

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Title

**24: Current Measurement**

Size

Document Number

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